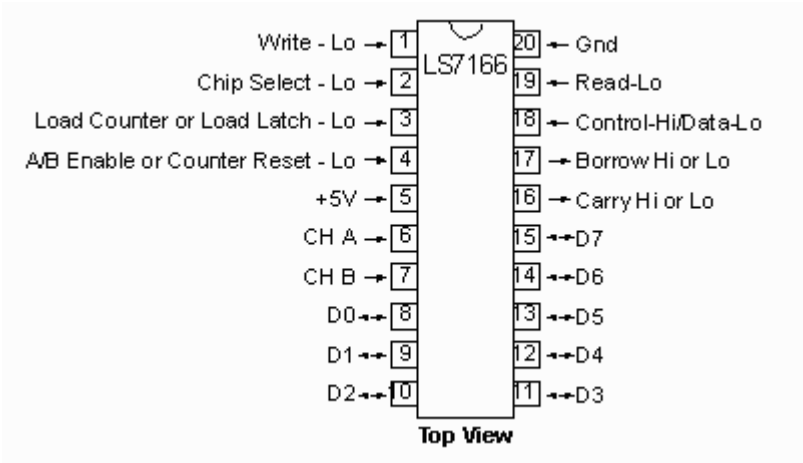
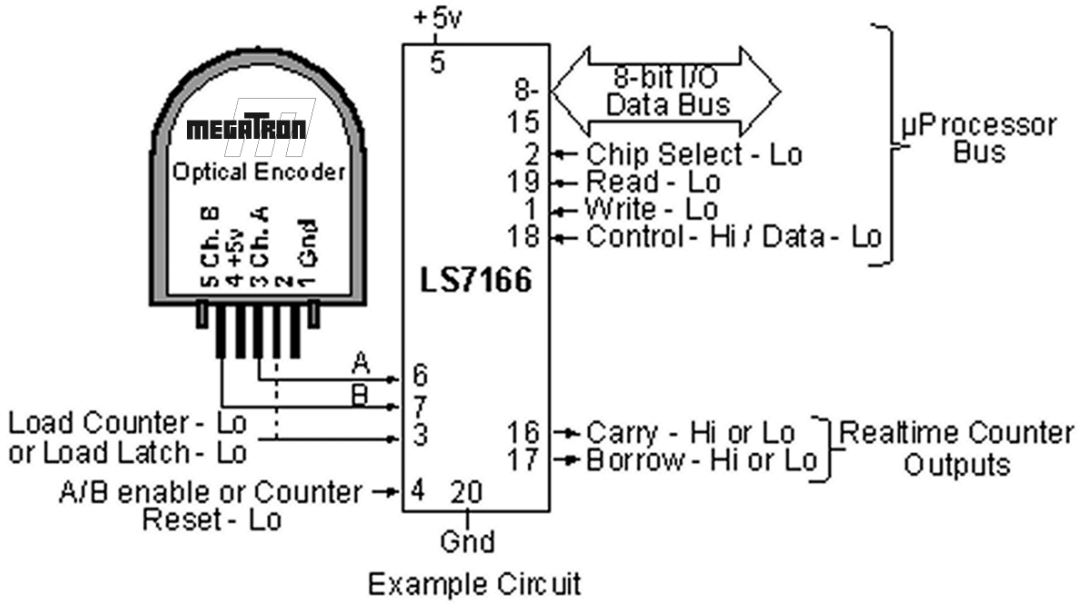
LS7166
Detailed Information

Pin Descriptions





Example Circuit

Realtime Hardware Input Pin Descriptions

A & B (Inputs) (Pins 6 & 7):
Connect to A & B quadrature outputs of the encoder. The quadrature code will be decoded and used to clock and steer the 24-bit Counter. It can be programmed to generate one clock once per quadrature cycle, once per 1/2 cycle or once per 1/4th cycle (X1, X2 or X4 mode). Max count frequency is 10 MHz.

A/B Enable or Counter Reset (Input) (Pin 4):
Active low. Minimum low pulse width is 60nSec. The function of this pin is defined by bit-4 of the Input Control Register. When bit-4 is low, a low level on this pin will reset the 24-bit counter. When bit-4 is high, a low level on this pin will enable the A & B inputs.

Load Counter or Load Latch (Input) (Pin 3):
Active low. Minimum low pulse width is 60ns. The function of this pin is defined by bit-5 of the Input Control Register. When bit-5 is low, a low level on this pin will transfer the contents of the 24-bit Preset Register to the 24-bit Counter. When bit-5 is high, a low level on this pin will transfer the contents of the 24-bit Counter to the 24-bit Counter Output Latch.

Microprocessor Bus Pin Descriptions

Data Bus (Pins 8-15):
Three-state, 8-bits. Used to pass data to and from the internal registers in single and multiple-byte transfers. Bits 6 & 7 are used as address bits to select the desired control registers during write operations.

Chip Select (Input) (Pin 2):
Active Low, enables the chip to Read or Write on the data bus.
Read (Input) (Pin 19):
Active Low, enables the Status Register or 1-byte of the 24-bit Output Latch to be read on the data bus.
Write (Input) (Pin 1):
Active Low, during chip select, latches the data bus into the internal registers.
Control-Hi/Data-Lo (Input) (Pin 18):
Used to address various resistors during read and write cycles. A high level during a read cycle selects the Status Register. A high level during a write cycle selects 1 of the 4 Control Registers. A low level during a write cycle selects one byte of the Preset Register. A low level during a read cycle selects one byte of the Counter Output Latch.

Realtime Hardware Output Pin Descriptions

Carry or Match (Output) (Pin 16): The function of this pin is defined by bits 4 and 5 of the Output Control Register as follows:

Bit-5	Bit-4	Pin Function
0	0	Carry - low true
0	1	Carry toggle flip flop (starts out low)
1	0	Carry - high true
1	1	24-bit Comparator / Counter match - low true

Borrow or Match (Output) (Pin 17): The function of this pin is also defined by bits 4 and 5 of the Output Control Register as follows:

Bit-5	Bit-4	Pin Function
0	0	Borrow - low true
0	1	Borrow toggle flip flop (starts out low)
1	0	Borrow - high true
1	1	24-bit Comparator/Counter match - toggle output

Note that the functions of pins 16 and 17 are defined by the same 2 bits of the Output Control Register. They are inseparably linked together.
The toggle flip flops are triggered by the trailing edges of the associated Carry, Borrow, or Compare match. Thus there is a 1-clock delay between the input and output of each flip flop. Unless otherwise specified, assume the longest prop delay from any input to any output is <110ns.

Register Descriptions

Register Access

Writing to 1 of the 4 Control Registers: Set Control/Data high. Bits 6 & 7 are used as address bits to select one of these 4 registers. Only bits 0-5 are stored.

D7	D6	C/D	RD	WR	CS	Function
X	X	X	X	X	1	Disable Chip for Read or Write
0	0	1	1		0	Write to Master Control Register
0	1	1	1		0	Write to Input Control Register
1	0	1	1		0	Write to Output Control Register
1	1	1	1		0	Write to Quadrature Control Register
X	X	0	1		0	Write to Preset Register, then increment Address Counter
X	X	0		1	0	Read Output Latch, then increment Address Counter
X	X	1		1	0	Read Output Status Register

Notes: D7 & D6 are the most significant bits of the data bus.
C/D is Control/Data pin 18.
RD is Read pin 19.
WR is Write pin 1.
CS is Chip Select pin 2.
X means "don't care".
Write Cycle Timing: Allow at least 15ns setup time for valid data, Chip Select and Control/Data before asserting Write. Make the write pulse at least 60ns long. Hold the data bus, Chip Select and Control/Data stable at least 50ns after deasserting Write.
Read Cycle Timing: The data bus will become valid within 110ns after asserting Chip Select, Control/Data and Read.

Status Register (Read only, Control)

Bit-0: Borrow Toggle Flip-Flip. Toggles every time the 24-bit counter underflows generating a borrow.
Bit-1: Carry Toggle Flip-Flip. Toggles every time the 24-bit counter overflows generating a carry. Trailing edge triggered.
Bit-2: Compare Toggle Flip Flop. Toggles every time the 24-bit counter equals the 24-bit Preset Register. Trailing edge triggered.
Bit-3: Sign bit. Set low when a Borrow occurs. Set high when a Carry occurs. Level triggered.
Bit-4: Up/Down Counter Direction. Reset low when counting down, Set high when counting up. Leading edge triggered.
Bits 5, 6 and 7 are always high.

Preset Register (Write Only, Data)

The 24-bit Preset Register is the input port for the 24-bit counter. The data is first written into the Preset Register in 3 write cycles (least significant byte 1st). The address pointer is automatically incremented with each write cycle.

Sequence:
• Reset the address pointer by setting bit-0 of the Master Control Register high. • Load byte 0 (LSB) into this register & increment address • Load byte 1 into this register & increment address • Load byte 2 (MSB) into this register & increment address • Transfer the 3-byte Preset Register to the 24-bit counter by setting bit-3 high of the Master Control Register.

Input Control Register (Write Only)

Defines the operating mode of this chip. Select this register by making bit-6 high and bit-7 low.
Bit 0: Single Cycle count setup. When bit-0 is low Input-A is up count and Input-B is down count. When bit-0 is high Input-A is count input and Input-B is count direction, where B=0 selects up count mode and B=1 selects down count mode. (Overridden in Quadrature mode)
Bits, 1 & 2: These bits must be reset low for normal operation.
Bit-3: Reset low to disable the A & B inputs. Set high to enable the A & B inputs.
Bit-4: The function of hardware pin 4 is defined by this bit. When bit-4 is low, a low level on pin 4 will reset the 24-bit counter. When bit-4 is high, a high level on pin 4 will disable the A & B inputs.
Bit-5: The function of hardware pin 3 is defined by this bit. When bit-5 is low, a low level on pin 3 will transfer the contents of the 24-bit Preset Register to the 24-bit Counter.
When bit-5 is high, a low level on pin 3 will transfer to contents of the 24-bit Counter to the 24-bit Counter Output Latch.

Output Control Register (Write Only)

Initializes the 24-bit Counter and sets operating modes. Select this register by making bit-6 low and bit-7 high. Control functions may be combined.
Bit-0: Low level selects binary count mode. High level selects BCD count mode.
Bit-1: This bit must be reset low for normal operation.
Bit-2: Low level selects normal wraparound count mode. High level selects divide-by-N mode (24-bit counter is reloaded from the Preset Register upon Carry or Borrow).
Bit-3: This bit must be reset low for normal operation.
Bits 4 & 5: The functions of hardware pins 16 & 17 are defined by these two bits. Pin 16 can be defined as any of the following:

Bit-5	Bit-4	Pin 16 Function
0	0	Carry - low true
0	1	Carry toggle flip flop (starts out low)
1	0	Carry - high true
1	1	24-bit Comparator/Counter match - low true

Pin 17 is also defined the the same two bits as follows:

Bit-5	Bit-4	Pin 17 Function
0	0	Borrow - low true
0	1	Borrow toggle flip flop (starts out low)
1	0	Borrow - high true
1	1	24-bit Comparator/Counter match - toggle output

Counter Output Latch (Read Only, Data)

The 24-bit counter value at any instant can be accessed by transferring its contents to the 24-bit Counter Output Latch. Note that only good stable data will be passed from the counter to the Output Latch even if the counter bits are in the midst of a transition. This chip will internally stretch the latch pulse if necessary until the counter has stabilized. The 3 bytes are then read from the Output Latch (least significant byte 1st). The address pointer is automatically incremented with each read cycle.

Sequence:
• Reset the Address Pointer and transfer the Counter value to the Output Latch by setting bits 0 and 1 of the Master Control Register high. These bits will automatically reset to zero after the Read Sequence. • Read byte 0 (LSB) and increment address • Read byte 1 and increment address • Read byte 2 (MSB) and increment address

Master Control Register (Write Only)

Performs register reset and load operations. Select this register by making bits 6 and 7 low. Writing a nonzero byte to this register does not require a follow-up write of an all-zeros byte to terminate an operation. Control functions may be combined. All bits are high true.
Bit-0: Reset the 3-byte Address Pointer, in preparation for a 3-byte (24-bit) write sequence of the Preset Register or read sequence of the Output Latch.
Bit-1: Transfer the 24-bit Counter contents to the 24-bit Output Latch.
Bit-2: Reset the 24-bit Counter, the Borrow Toggle Flip-Flop and the Carry Toggle Flip-Flop and set the Sign bit high.
Bit-3: Transfer the 24-bit Preset Register to the 24-bit Counter.
Bit-4: Reset the Comparator Match Toggle Flip-Flop.
Bit-5: Master Reset. Reset the 24-bit Counter, the Input Control Register, the Output Control Register, the Quadrature Register, the Borrow Toggle Flip-Flop, the Carry Toggle Flip-Flop, the Comparator Toggle Flip-Flop and the 3-byte address pointer. Note: Master reset does not reset the counter perfectly. The counter will be either 1, 0 or -1 after a master reset. To reliably reset the counter to 0, do a Reset Counter Command with bit-2 as shown above.

Quadrature Control Register (Write Only)

Selects the quadrature count mode. Select this register by making bit-6 high and bit-7 high. It can be programmed to generate one clock once per quadrature cycle, once per 1/2 cycle or once per 1/4th cycle (X1, X2 or X4 mode). For example, a 500 cycle/rev encoder can provide 500, 1000 or 2000 counts/rev.

Bit-1	Bit-0	Quadrature Count Mode
0	0	Not valid
0	1	X1 mode
1	0	X2 mode
1	1	X4 mode

Bits-3 & 5: These bits do not matter.

LS7166
Sample C Source Code

```
/* LS7166 APPLICATION NOTE */
/* note: pin 3 and pin 4 are normally high, pin 18 to address 0 */
/* Borland C source code */

#include "stdio.h"
#include "dos.h"
#include "conio.h"

/* addresses */
#define BASE            0X300                   // base address of
interface board
#define DATA1           BASE+0                  // data register of LS7166
#define CONTROL1        BASE+1                  // control register of
LS7166
#define LOAD            BASE+8                  // a write toggles pin 3 of
LS7166

/* LS7166 commands */
#define MASTER_RESET  0X20                      // master reset command
#define INPUT_SETUP   0X68                      // setup counter input mode
#define QUAD_X1       0XC1                      // quadrature multiplier to
1
#define QUAD_X2       0XC2                      // quadrature multiplier to
2
#define QUAD_X4       0XC3                      // quadrature multiplier to
4
#define ADDR_RESET    0X01                      // reset address pointer
#define LATCH_CNTR    0X02                      // latch counter
#define CNTR_RESET    0X04                      // reset counter
#define PRESET_CTR    0X08                      // transfer preset to
counter

void init(void) {                                       // initialize the
7166
        outportb(CONTROL1, MASTER_RESET);
        outportb(CONTROL1, INPUT_SETUP);
        outportb(CONTROL1, QUAD_X4);
        outportb(CONTROL1, CNTR_RESET);
        /* preset counter to 44 */
        outportb(CONTROL1, ADDR_RESET); // reset addr
        outportb(DATA1, 0x44);                  // output preset value
        outportb(DATA1, 0x0);                   // output preset value
        outportb(DATA1, 0x0);                   // output preset value
        outportb(CONTROL1, PRESET_CTR); // preset to counter
}

void soft_latch(void) {                         // latch position with
software command
        outportb(CONTROL1, LATCH_CNTR); // counter to latch
}

void hard_latch(void) {                         // latch position with low
pulse on pin 3
        outportb(LOAD, 0);                      // toggle pin 3 of LS 7166
}

long read_position(void) {                      // read position of encoder
        long position;
```

```
        outportb(CONTROL1, ADDR_RESET); // reset address pointer
        position  = (long)inportb(DATA1);              // least
significant byte
        position += (long)inportb(DATA1) << 8;
        position += (long)inportb(DATA1) <<16;  // most significant byte
        return position;
}
void main(void) {
        init();
        while (!kbhit()) {
        soft_latch();
        printf("\n position =%8lX", read_position());
}
```

Assembly Source Code

```
.DATA
position                DB      0,0,0   ; 3 byte position

; Addresses
BASE                    EQU     0X300   ; base address of interface board
DATA1                   EQU     BASE+0  ; data register of LS7166
CONTROL1        EQU     BASE+1  ; control register of LS7166
LOAD                    EQU     BASE+7  ; a write toggles pin 3 of LS7166

; LS7166 commands
MASTER_RESET    EQU     0X20    ; master reset command
INPUT_SETUP     EQU     0X68    ; setup counter input mode
QUAD_X1         EQU     0XC1    ; setup quadrature multiplier to 1
QUAD_X2         EQU     0XC2    ; setup quadrature multiplier to 2
QUAD_X4         EQU     0XC3    ; setup quadrature multiplier to 4
ADDR_RESET      EQU     0X01    ; reset address pointer
LATCH_CNTR      EQU     0X02    ; latch counter
CNTR_RESET      EQU     0X04    ; reset counter
PRESET_CTR      EQU     0X08    ; transfer preset register to counter

.CODE
move    ax,@data
move    ds,ax                   ; ds to point to data segment

; initialize the LS7166
mov     dx,CONTROL1
mov     al,MASTER_RESET
out     dx,al                   ; send master reset command
mov     al,INPUT_SETUP
out     dx,al                   ; send counter input mode command
mov     al,QUAD_X4
out     dx,al                   ; setup quadrature multiplier to 4
mov     al,CNTR_RESET
out     dx,al                   ; reset counter


; transfer counter to latch
mov     dx,CONTROL1
mov     al,LATCH_CNTR
out     dx,al

; reset address pointer
mov     dx,CONTROL1
mov     al,ADDR_RESET
out     dx,al
```

```
; read position of encoder
mov     dx,DATA1
mov     bx,OFFSET position
```